REMARKS

Claims 80, 84, 88, 93, 97, 102, and 106 are amended. Claims 1-79 are canceled. The amendment and cancelation of claims is made without prejudice.

Claim 80 stands objected to for informalities. In view of the amendment, this objection is moot.

Claims 80-96, 102-104, and 106 stand rejected under 35 U.S.C. § 102(e) as anticipated by U.S. Patent 6,977,684 ("Hashimoto"). Applicant respectfully traverses this rejection.

Claim 80 defines a method of operating an active pixel CMOS imager and recites "activating a first address circuit for a first pixel of a pixel array and a second address circuit for a second pixel adjacent to said first pixel, said first pixel and said second pixel being in a row of pixels, said first address circuit consisting of a first row select line and a shared column line, and said second address circuit consisting of a second row select line and said shared column line; activating at least one of the first row select line and the second row select line, wherein the first row select line and the second row select line each run along the row of pixels and are not connected to pixels of any other row of the array; and generating an output signal over the shared column line corresponding to charge accumulated by at least one of the first pixel and second pixel." Such a method is not anticipated by Hashimoto.

Every embodiment of Hashimoto requires at least two row lines, i.e., a row select line (e.g., 60) and a scanning line (e.g., 59), and a column line, i.e., vertical signal line (e.g., 57), as an addressing circuit. This is exemplified by Hashimoto Figs. 5 and 9, reproduced below:

FIG. 5

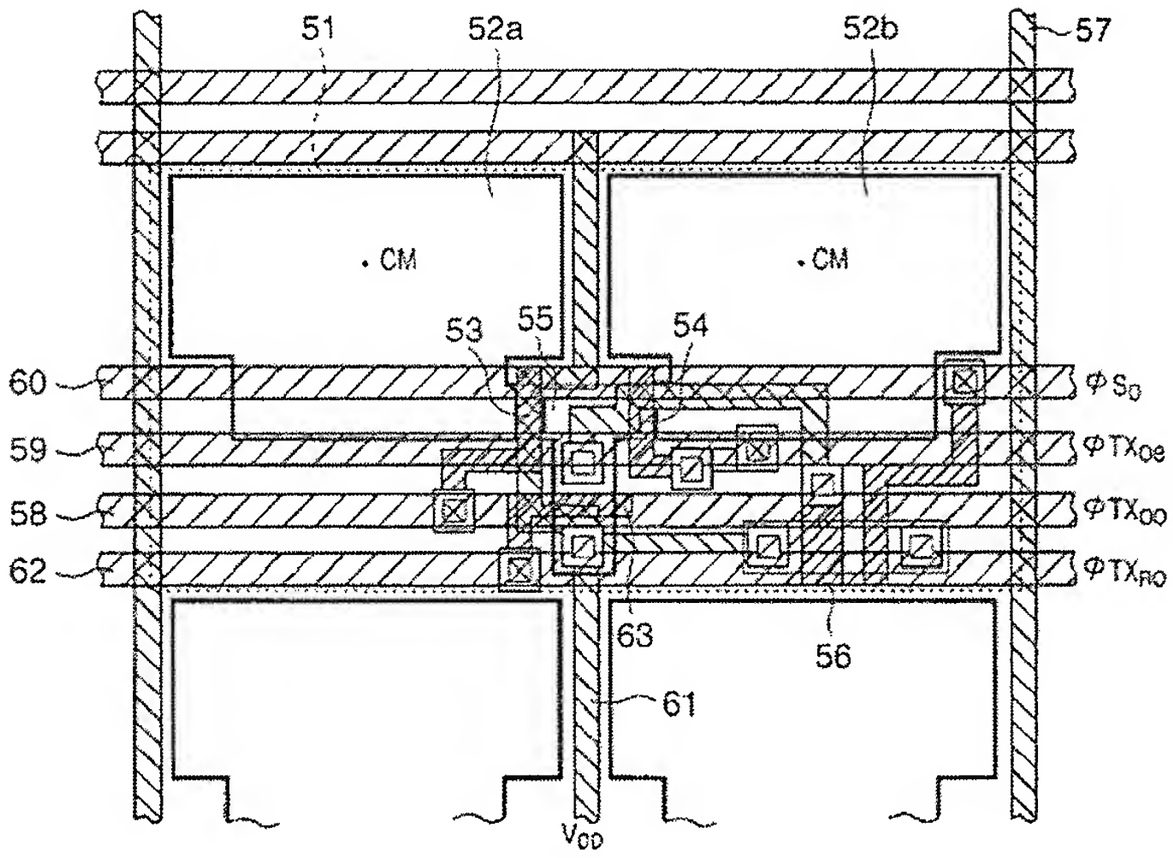
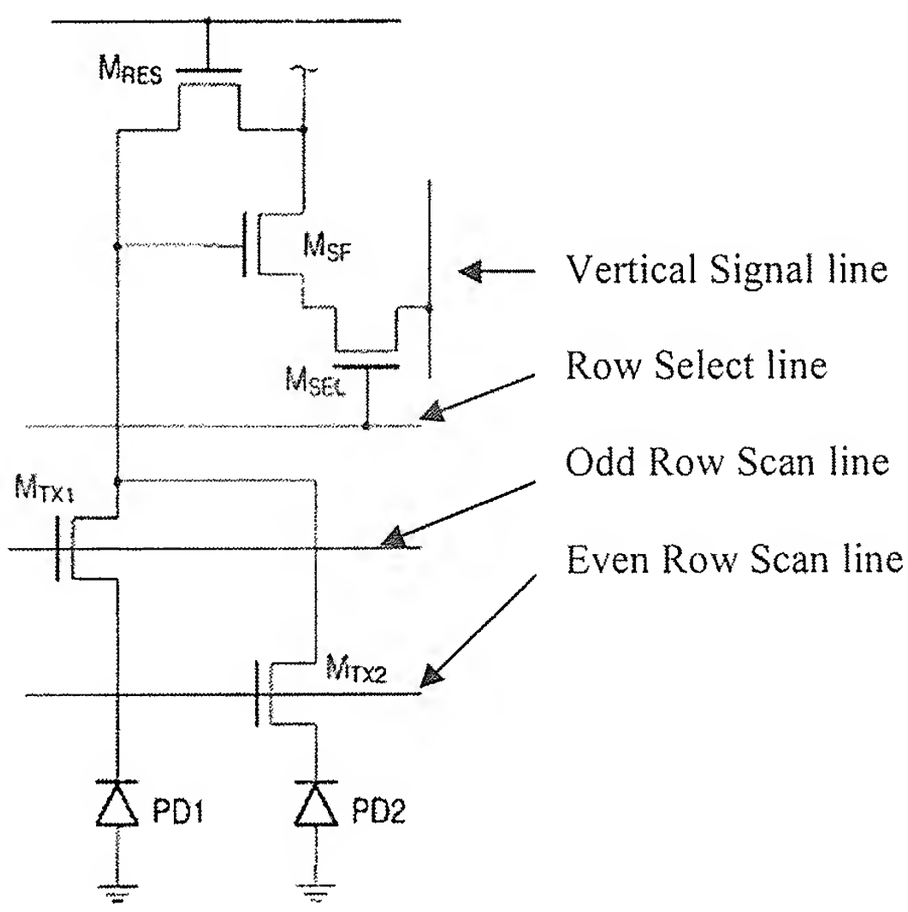


FIG. 9



The Hashimoto address circuit for the disclosed two-dimensional imaging array (to read pixels) is explained throughout the Hashimoto disclosure as requiring the vertical signal line, an odd row scanning line, an even row scanning line, and a row selection line. *See*, *inter alia*, Hashimoto col. 5, ll. 42-45; col. 6, ll. 45-48; col. 9, ll. 43-52; and col. 10, ll. 6-26. Hashimoto's address circuit is, therefore, different from that defined by the claim. Hashimoto fails to disclose "activating a first address circuit for a first pixel of a pixel array and a second address circuit for a second pixel adjacent to said first pixel, said first pixel and said second pixel being in a row of pixels, said first address circuit consisting of a first row select line and a shared column line, and said second address circuit consisting of a second row select line and said shared column line; activating at least one of the first row select line and the second row select line, wherein the first row select line and the second row select line each run along the row of pixels and are not connected to pixels of any other row of the array," as recited by independent claim 80.

Because Hashimoto fails to disclose each feature of the claimed method, independent claim 80 and dependent claims 81-83 are not anticipated by the reference. Applicant respectfully requests that the 35 U.S.C. § 102(e) rejection of these claims be withdrawn and the claims allowed.

Claim 84 defines a method of operating a system and recites "focusing an image on an active pixel CMOS imager, the imager comprising a pixel array; activating a first address circuit for a first pixel of a pixel array and a second address circuit for a second pixel adjacent to said first pixel, said first pixel and said second pixel being in a row of pixels, said first address circuit consisting of a first row select line and a shared column line, and said second address circuit consisting of a second row select line and said shared column line; addressing the first pixel using the first row select line and then subsequently addressing the second pixel using the second row select line, the first row select line and second row select line each running along the length of the row and not being connected to pixels of any other row; resetting a voltage level of a node associated with the first pixel to a predetermined voltage using a reset transistor addressed by a reset line that extends approximately linearly across the pixel array; transferring charge collected by the first pixel to the node; detecting the charge at the node; and generating an output signal over the shared column line, the output signal corresponding to the image." This method is not anticipated by Hashimoto.

Similar to independent claim 80, independent claim 84 recites "activating a first address circuit for a first pixel of a pixel array and a second address circuit for a second pixel adjacent to said first pixel, said first pixel and said second pixel being in a row of pixels, said first address circuit consisting of a first row select line and a shared column line, and said second address circuit consisting of a second row select line and said shared column line." As discussed above, Hashimoto's addressing circuitry for its two-dimensional pixel array is different.

Because Hashimoto fails to disclose each feature of the claimed method, independent claim 84 and dependent claims 85-87 are not anticipated by the reference. Applicant respectfully requests that the 35 U.S.C. § 102(e) rejection of these claims be withdrawn and the claims allowed.

Claim 88 defines an active pixel CMOS imager and recites "a plurality of pixels to generate an output signal associated with detected light, the plurality of pixels arranged in rows and columns of an array, each said row having both odd and even pixels, wherein each said odd pixel is addressed by a respective first address circuit consisting essentially of an odd row select line and a shared column line, and wherein each said even pixel is addressed by a respective second address circuit consisting essentially of an even row select line and a shared column line, wherein the even row select lines do not address the odd pixels and the odd row select lines do not address the even pixels; a plurality of column lines comprising the column lines of the first address circuit and the second address circuit, each of the plurality of column lines being connected to at least two adjacent pixels of a row in the array, the column lines being connected to output circuitry to output the signal; a column driver to address pixels connected to the column lines; and a row driver to address pixels through the odd row select lines and the even row select lines." This device is not disclosed by Hashimoto.

Similar to independent claim 80, independent claim 88 recites "each said odd pixel is addressed by a respective first address circuit consisting essentially of an odd row select line and a shared column line, and wherein each said even pixel is addressed by a respective second address circuit consisting essentially of an even row select line and a shared column line, wherein the even row select lines do not address the odd pixels and the odd row select lines do not address the even pixels." As discussed above, Hashimoto's addressing circuitry for its two-dimensional pixel array is different.

Because Hashimoto fails to disclose each feature of the claimed device, independent claim 88 and dependent claims 89-92 are not anticipated by the reference. Applicant respectfully requests that the 35 U.S.C. § 102(e) rejection of these claims be withdrawn and the claims allowed.

Claim 93 defines a method of operating a CMOS imager and recites "providing a first address circuit for even pixels of row of pixels and a second address circuit for odd pixels of the row of pixels, said first address circuit consisting essentially of an even row select line and a plurality of

shared column lines, and said second address circuit consisting essentially of an odd row select line and said plurality of shared column lines, wherein the even row select lines do not address the odd pixels and the odd row select lines do not address the even pixels; addressing the even pixels using a row driver coupled to the even row select line; providing a first output signal associated with light detected by the even pixels to the plurality of shared column lines; addressing the odd pixels using the row driver coupled to the odd row select line; and providing a second output signal associated with light detected by the odd pixels to the plurality of shared column lines." This method is not disclosed by Hashimoto.

Similar to independent claim 80, independent claim 93 recites "providing a first address circuit for even pixels of row of pixels and a second address circuit for odd pixels of the row of pixels, said first address circuit consisting essentially of an even row select line and a plurality of shared column lines, and said second address circuit consisting essentially of an odd row select line and said plurality of shared column lines, wherein the even row select lines do not address the odd pixels and the odd row select lines do not address the even pixels." As discussed above, Hashimoto's addressing circuitry for its two-dimensional pixel array is different.

Because Hashimoto fails to disclose each feature of the claimed method, independent claim 93 and dependent claims 94-96 are not anticipated by the reference. Applicant respectfully requests that the 35 U.S.C. § 102(e) rejection of these claims be withdrawn and the claims allowed.

Claim 102 defines an imaging device and recites "a pixel array comprising a row of first pixels and second pixels; a first address circuit for the first pixels consisting essentially of a first row select line and a plurality of shared column lines; a second address circuit for the second pixels consisting essentially of a second row select line and said plurality of shared column lines, wherein the first row select lines do not address the second pixels and the second row select lines do not address the first pixels, each of the shared column lines being associated with a first pixel and a second pixel; and a reset line connected to the first pixels." This device is not disclosed by Hashimoto.

Similar to independent claim 80, independent claim 102 recites "a first address circuit for the first pixels consisting essentially of a first row select line and a plurality of shared column lines; a second address circuit for the second pixels consisting essentially of a second row select line and said plurality of shared column lines, wherein the first row select lines do not address the second pixels and the second row select lines do not address the first pixels." As discussed above, Hashimoto's addressing circuitry for its two-dimensional pixel array is different.

Because Hashimoto fails to disclose each feature of the claimed device, independent claim 102 and dependent claims 103-104 are not anticipated by the reference. Applicant respectfully requests that the 35 U.S.C. § 102(e) rejection of these claims be withdrawn and the claims allowed.

Claim 106 defines an imaging device and recites "a row of pixels comprising a first plurality of pixels and a second plurality of pixels; a first address circuit for the first plurality of said pixels and a second address circuit for the second plurality of said pixels, said first address circuit consisting essentially of a first row select line and a plurality of shared column lines, and said second address circuit consisting essentially of a second row select line and said plurality of shared column lines, wherein the first row select lines do not address the second plurality of pixels and the second row select lines do not address the first plurality of pixels, each of said plurality of shared column lines being connected to a first pixel of the first plurality of pixels and a second pixel of the second plurality of pixels; and a reset line connected to at least the first plurality of pixels or the second plurality of pixels." This device is not disclosed by Hashimoto.

Similar to independent claim 80, independent claim 106 recites "a first address circuit for the first plurality of said pixels and a second address circuit for the second plurality of said pixels, said first address circuit consisting essentially of a first row select line and a plurality of shared column lines, and said second address circuit consisting essentially of a second row select line and said plurality of shared column lines, wherein the first row select lines do not address the second plurality of pixels and the second row select lines do not address the first plurality of pixels."

As discussed above, Hashimoto's addressing circuitry for its two-dimensional pixel array is different.

Because Hashimoto fails to disclose each feature of the claimed device, independent claim 106 is not anticipated by the reference. Applicant respectfully requests that the 35 U.S.C. § 102(e) rejection of this claim be withdrawn and the claim allowed.

Claims 97-101 and 105 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Hashimoto in view of U.S. Patent 6,130,423 ("Brehmer"), U.S. Patent 5,721,422 ("Bird"), and U.S. Patent 5,587,738 ("Shinohara"). Applicant respectfully traverses this rejection.

Claim 97 defines an imaging device and recites "a row comprising a first pixel and a second pixel; the first and second pixels being joined by a diagonal active area component; a first even row line connected with the first pixel; a second odd row line connected with the second pixel, wherein said first even row line and said second odd row line are associated with said row and not any other row; a column line connected with the first and second pixels at the diagonal active area component; a first address circuit for the first pixel consisting essentially of the first even row select line and a shared column line; and a second address circuit for the second pixel consisting essentially of the second odd row select line and said shared column line, wherein the first even row select line does not address the second pixel and the second odd row select line does not address the first pixel." This device is not taught or suggested by the Hashimoto-Brehmer-Bird-Shinohara combination.

Similar to independent claim 80, independent claim 97 recites "a first address circuit for the first pixel consisting essentially of the first even row select line and a shared column line; and a second address circuit for the second pixel consisting essentially of the second odd row select line and said shared column line, wherein the first even row select line does not address the second pixel and the second odd row select line does not address the first pixel." As discussed above, Hashimoto's addressing circuitry for its two-dimensional pixel array is different and the claimed

feature is not taught or suggested by the primary reference. Likewise, this feature is not taught or suggested by any of the other cited references – Brehmer, Bird, and Shinohara – nor is such a teaching or suggestion alleged to be provided by any of these references in the Office action. Therefore, the cited combination fails to teach or suggest each feature of the claimed subject matter.

Because the Hashimoto-Brehmer-Bird-Shinohara combination fails to teach or suggest each feature of the claimed device, independent claim 97 and dependent claims 98-101 are patentable over the cited combination. Applicant respectfully requests that the 35 U.S.C. § 103(a) rejection of these claims be withdrawn and the claims allowed.

Claim 105 depends from independent claim 102, which is discussed above as patentable over Hashimoto individually. Likewise, independent claim 102 and dependent claim 105 are patentable over the Hashimoto-Brehmer-Bird-Shinohara combination since the combination does not teach or suggest "a first address circuit for the first pixels consisting essentially of a first row select line and a plurality of shared column lines; a second address circuit for the second pixels consisting essentially of a second row select line and said plurality of shared column lines, wherein the first row select lines do not address the second pixels and the second row select lines do not address the first pixels," as recited by independent claim 102.

Because the Hashimoto-Brehmer-Bird-Shinohara combination fails to teach or suggest each feature of the claimed device, claim 105 is patentable over the cited combination. Applicant respectfully requests that the 35 U.S.C. § 103(a) rejection of this claim be withdrawn and the claim allowed.

In view of the above, Applicant believes the pending application is in condition for allowance. A notice of allowance for all pending claims, 80-106, is respectfully requested.

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Respectfully submitted,

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